Nano-CMOS Design for Manufacturability: Robust Circuit and Physical Design for Sub-65nm Technology Nodes
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DESCRIPTION

Discover innovative tools that pave the way from circuit and physical design to fabrication processing

Nano-CMOS Design for Manufacturability examines the challenges that design engineers face in the nano-scaled era, such as exacerbated effects and the proven design for manufacturability (DFM) methodology in the midst of increasing variability and design process interactions. In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore’s law, the authors also tackle complex issues in the design process to overcome the difficulties, including the use of a functional first silicon to support a predictable product ramp. Moreover, they introduce several emerging concepts, including stress proximity effects, contour-based extraction, and design process interactions.

This book is the sequel to Nano-CMOS Circuit and Physical Design, taking design to technology nodes beyond 65nm geometries. It is divided into three parts:

- Part One, Newly Exacerbated Effects, introduces the newly exacerbated effects that require designers’ attention, beginning with a discussion of the lithography aspects of DFM, followed by the impact of layout on transistor performance
Part Two, Design Solutions, examines how to mitigate the impact of process effects, discussing the methodology needed to make sub-wavelength patterning technology work in manufacturing, as well as design solutions to deal with signal, power integrity, WELL, stress proximity effects, and process variability.

Part Three, The Road to DFM, describes new tools needed to support DFM efforts, including an auto-correction tool capable of fixing the layout of cells with multiple optimization goals, followed by a look ahead into the future of DFM.

Throughout the book, real-world examples simplify complex concepts, helping readers see how they can successfully handle projects on Nano-CMOS nodes. It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and, in short, make designs that are not only functional, but that also meet power and performance goals within the design schedule.

ABOUT THE AUTHOR

Ban P. Wong, CEng, MIET, is Director of Design Methodology at Chartered Semiconductor, Inc. He holds five patents and is the lead author of Nano-CMOS Circuit and Physical Design (Wiley).

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Victor Moroz, PhD, is a Principal Engineer at Synopsys. He focuses on semiconductor physics, including silicon process integration, teaching undergraduate and graduate students, and developing process simulation and DFM tools.

Anurag Mittal, PhD, Yale University, has co-developed the world's first truly CMOS-compatible Flash technology. He has several papers, invited talks, and patents to his credit. Currently he is Director of Technology & Applications at Takumi Inc., where he is developing novel EDA solutions on Design for Variability & Reliability.

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